University of Arkansas Microelectronics-Photonics Graduate Program
PhD Candidacy Exam – March 15, 2002
Materials and Processing Area of Emphasis Exam

You are a senior development engineer for a major microelectronics manufacturer. The company has initiated an R&D program on the idea of stacking a memory chip and a microprocessor chip, face-to-face for maximum speed. The anticipated market for this configuration of product in first stage production would be 5000 stacked chip systems per day.

The microprocessor chip is 14 x 14 mm and the memory chip is 8 x 8 mm. Both chips are 20 mils thick.

The microprocessor chip has 160 four-mil pads, which must all be connected to the board. There are an additional 64 four-mil pads that are used for connectivity to the memory chip. With this new packaging configuration, the microprocessor pad placement can be modified from the traditional peripheral layout if advantageous to the total solution.

The memory chip has 64 four-mil pads equally spaced around the periphery, which will all mate to corresponding 64 four-mil pads on the microprocessor.

Some specifications on the chips and circuit board:

- All pads on both chips are Al.
- The passivation on both chips is silicon nitride.
- The microprocessor requires 30 W of power, and the memory chip requires 5 W.
- The board will be FR4 with 1/2 oz. Cu metallization.
- The unit will operate in normal office ambient temperature of about 25 deg C.
- Maximum junction temperature is 70 deg C.

When describing your investigations of the following items, always describe what you consider to be the optimal solution to the problem and fully describe the technical elements that affected your decision. If alternative approaches exist, neither of which is strongly advantageous over the other, then discuss both approaches with the pros and cons of each approach (but even in this case, you must identify the approach you recommend that your group pursue).

Part A (must be answered):

Describe with a high level of technical detail the configuration of the total operating system you envision that contains the two chips and the board relative to one another, any kind of chip packaging that will be used, and any other unusual system elements that might be required to support your solution. Your design should consider all the aspects of effective packaging: mechanical, environmental, thermal, electrical etc.

Evaluate candidate configurations and materials for chip-to-chip attachment, mounting the assembly on a board, electrically connecting the microprocessor to the board, etc. Specify and

size all parts and materials. Use off-the-shelf components and technology where possible. It is not required that the resulting assembly be hermetic.

Part B (address two of the four following items):

1. Describe the processing flow you would use to achieve this in some detail. This description should provide sufficient information that a first pass cost of manufacturing model could be built.
2. Design a testing regimen to evaluate the proposed process and materials to ensure mechanical and electrical reliability. This should include full characterization and qualification testing of the system for customer qualification and acceptance, as well as the testing that would be put in place to assure customer satisfaction during full production.
3. Demonstrate that the maximum junction temperature is not exceeded anywhere in the system at the specified operating condition. Fully describe your assumptions concerning the two chips' design layouts that impacted your analysis.
4. Describe the cost of manufacturing this product in first stage production manufacturing. You may exclude from your analysis possible additional costs in such infrastructure areas as human resources, facilities engineering, janitorial and grounds, upper level management, etc. You must include all direct manufacturing costs, both startup and continuing; and you must discuss explicitly space and personnel requirements to set up this stand-alone product line. You may exclude the cost of the microprocessor and memory chips from your calculations.

Part C (must be answered):

Consider the intellectual property content of your solution described in Part A. Determine if there are any existing IP public disclosures that would restrict implementation of your solution, describing in detail the potential conflict of the three closest IP publications. List all IP sources you consulted while formulating your answer, and include the full list of examined documents as an appendix to this exam (the full list will not be counted as part of your 15 page limit).

Part D (must be answered):

The system you designed in Part A has been shipping from your factory for 24 months, and you are receiving some units back from customers with catastrophic and complete separation of the two chips. It is your task to perform failure analysis on the returned systems.

1. Describe the information you will seek from your customer base to help you determine the cause of the separation of the chips.
2. Propose the three most likely hypotheses explaining why the chips separated. Describe the analytical techniques and instruments you will use to investigate the cause of the chip separation, including the reasons these techniques/instruments are the most appropriate to help you clearly determine which of your three reasons for separation is the correct hypothesis.

Part E (must be answered): Your management team is concerned that the face-to-face chip packaging scheme may not meet your customer's needs. Evaluate the possibility of instead using optical communication between the chips mounted in a standard MCM substrate package to avoid having to place them in this face-to-face configuration. Consider both current and projected optical technologies. Determine how this would affect the distance requirement between the chips as compared to current metallic interconnects.

Your answer to Part E should be in the form of an upper level management white paper. It should contain sufficient detail to convince your management team of the merits of your analysis, and should be written with the objective of securing the necessary resources to support a detailed technical examination of the most favorable optical communication scheme identified in your report.